# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
# BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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| Appellant: | Yu |
| Filing Date: | January 3, 2000 |
| For: | MOS TRANSISTOR WITH ASYMMETRICAL SOURCE/ DRAIN EXTENSIONS |
| Group Art Unit: | 2815 |
| Docket No.: | 39153/223 |
| Application No.: | 09/476,961 |
| Examiner: | Warren, M. |

**CERTIFICATE OF EXPRESS MAILING**
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*EL 979078193 US* (Express Mail Label Number) *January 27, 2004* (Date of Deposit)

*Jean M. Tibbetts* (Printed Name)

Jean M. Tibbetts (Signature)



## BRIEF ON APPEAL

**Mail Stop – APPEAL BRIEF - PATENTS**
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

This paper is being filed in response to the final Office Action dated July 28, 2003 (finally rejecting Claims 18, 21-25 and 28-37). The Notice of Appeal was filed on October 27, 2003. Appellant respectfully requests reconsideration of the application.

Under the provisions of 37 CFR 1.192, this Appeal Brief is being filed in triplicate together with a check in the amount of $330.00 covering the Rule 17(c) Appeal Fee. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 06-1447.

## REAL PARTY IN INTEREST

This application was assigned to Advanced Micro Devices, Inc. having a place of business at One AMD Place, 1160 Kern Avenue, Sunnyvale, CA 94088.

## RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

1-29-04

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2815

Atty. Dkt. No. 039153-0223 (E0554)

*IN THE UNITED STATES PATENT AND TRADEMARK OFFICE*

Applicant: Yu

Title: MOS TRANSISTOR WITH ASYMMETRICAL SOURCE/DRAIN EXTENSIONS

Appl. No.: 09/476,961

Filing Date: 01/03/2000

Examiner: Warren, Matthew E.

Art Unit: 2815

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Jean M. Tibbetts
(Printed Name)

Jean M. Tibbetts
(Signature)



## TRANSMITTAL OF APPEAL BRIEF

Mail Stop – APPEAL BRIEF – PATENTS

Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

Transmitted herewith are the following documents for the above-identified application.

[ X ] Brief on Appeal (in triplicate, 14pages each).

[ X ] Petition for Extension of Time (1-mo. extension)

[ X ] Check No. 13576 in the amount of $440.00 (fee for filing Appeal Brief and 1-month extension of time).

The extension fee for response within the first month is $110.00. This amount has been added to and included in the total filing fee.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date 1/27/04

By Jean M. Tibbetts

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## STATUS OF THE CLAIMS

This is an appeal from the Final Office Action mailed July 28, 2003, finally rejecting Claims 18, 21-25 and 28-37 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,677,224 (Kadosh et al.) in view of U.S. Patent No. 5,625,216 (Miller). Claims 19 and 20 have been allowed. Claims 26 and 27 have been objected to as being dependent on a rejected base claim. Claims 18, 21-25 and 28-37 are the subject of the present appeal.

## STATUS OF THE AMENDMENTS

No amendment has been filed subsequent to the Final Office Action.

## SUMMARY OF THE INVENTION

The present invention relates to integrated circuits and in particular to a transistor having asymmetrical source/drain extensions and methods for manufacturing the same. (Specification, page 1, lines 12-15). As transistors disposed on integrated circuits become smaller, proper design and engineering of the source/drain extensions becomes critical to the operation of small-scale transistors. (Specification, page 2, lines 17-20). Asymmetrical source and drain extensions, in particular, a drain extension which is deeper than a source extension, provide advantageous transistor performance. (Specification, page 5, line 18 to page 6, line 11).

Claim 18, the representative claim for the first group, is directed to an integrated circuit including a plurality of transistors. Each of the transistors 12 includes a gate structure 18 disposed over a channel 31, a deep source region 22, a deep drain region 24, a source extension 23 and a drain extension 25. The deep source region 22 and the deep drain region 24 are heavily doped with dopants of a first conductivity type. (Figure 1, Specification, page 4, line 23 to page 5, line 3). Source extension 23 is integral to the deep source region 22 and drain extension 25 is integral to the deep drain region 24. The source extension 23 and the drain extension 25 are disposed partially underneath the gate structure 18 and are thinner than the deep source region 22 and the deep drain region 24. (Figure 1, Specification, page 5, lines 18-21 and page 5, line 30 to page 6, line 2). Drain extension 25 is deeper than the source extension 23. (Figure 1, Specification, page 5 line 17 to page 6 line 11).

Claim 31, the representative claim of the second group, is directed to an ultra-large scale integrated circuit including a plurality of transistors. (Specification, page 6, lines

12-14). Each transistor 12 includes a gate structure 12 on a top surface of a semiconductor substrate that is between a deep source region 22 and a deep drain region 24 with dopants of a first conductivity type. (Figure 1, Specification, page 4, line 23 to page 5, line 3). Each transistor 12 also includes a source extension 23 with dopants of the first conductivity type and a drain extension 25 with dopants of the first conductivity type. The drain extension 25 is deeper than the source extension 23. (Figure 1, Specification, page 5, line 17 to page 6, line 11).

Claim 36, the representative claim of the third group, is dependent upon claim 31. Claim 36 includes the additional feature of a unique concentration of dopants associated with the deep source and deep drain regions and the source extension and the drain extension. (Specification, page 4, line 30 to page 5, line 1, page 5, lines 25-26 and page 6, lines 10-11).

## ISSUES

1. Whether the claims of Groups 1-3 may properly be rejected under 35 U.S.C. § 103(a) based on Kadosh et al. (U.S. 5,677,224) in view Miller (US 5,625,216)?

## GROUPING OF THE CLAIMS

For the purposes of this appeal only, grouping of the claims is as follows:

1. Claims 18, 21-25 and 28-30 essentially stand or fall together and are therefore grouped together. Independent claim 18 is the representative claim for the group because it is the broadest claim in the group.

2. Claims 31-35 and 37 essentially stand or fall together and are therefore grouped together. Independent claim 31 is the representative claim for the group because it is the broadest claim in the group.

3. Claim 36 essentially stands or falls by itself and is therefore grouped by itself. Claim 36 depends from claim 31 and includes the additional feature of unique concentrations of dopants associated with the deep source region, the deep drain region, the source extension and the drain extension.

Thus, Appellant respectfully requests individual consideration of each of the three groups herein described. The separate patentability of groups 1-3 is discussed below in the Argument.

## ARGUMENT

### REFERENCES RELIED UPON

The following references were relied upon by the Examiner: U.S. Patent No. 5,677,224 to Kadosh et al., issued October 14, 1997 and U.S. 5,625,216 to Miller, issued April 29, 1997.

### BRIEF DESCRIPTION OF REFERENCES

1. U.S. Patent No. 5,677,224 to Kadosh et al. (hereinafter referred to as Kadosh) issued on October 14, 1997. Kadosh teaches a method for making asymmetrical N-channel and P-channel devices. One or both devices include a lightly doped drain region, heavily doped source and drain regions, and an ultra-heavily doped source region. (Kadosh, col. 3, lines 6-10). A heavily doped source region (P+) 204 and a ultra-heavily doped source region (P++) 206 merge to form a source and lightly doped drain region (P-) 152 and heavily doped drain region (P+) 198 merge to form a drain. (Kadosh, Figure 1U, col. 9, lines 40-57). Drain extension 152 is shallower than source extension 204. (Kadosh, Figure 1U). Such a device structure has low source-drain series resistance and reduces hot carrier effects. (Kadosh col. 3, lines 13-15).

2. U.S. Patent No. 5,625,216 to Miller (hereinafter referred to as Miller) issued on April 29, 1997. Miller teaches a MOS transistor and process for manufacturing a MOS transistor having a gate-drain underdiffusion length, $U_d$, that is longer than the gate-source underdiffusion length, $U_s$. (Miller, Abstract, Figure 6, col. 2, lines 1-7). The result is an increased gate-drain capacitance without providing a separate gate-drain capacitor and without requiring significant additional die area or critical mask alignment steps to form the capacitor. (Miller, Abstract, col. 1, lines 63-67 and col. 2, lines 26-31). The source and drain underdiffusion lengths, $U_s$ and $U_d$, are the overlap of gates 28 and the drain 27 and source 29, respectively. (Miller, Figures 1 and 6, col. 1, lines 29-32 and lines 34-37 and col.; 3, lines 57-62). The drain region 27 is provided with a p+ diffusion depth that achieves the desired underdiffusion length, $U_d$, and therefore the desired gate-drain capacitance. (Miller, Figure 6, col. 2, lines 15-19, col. 3, lines 9-17 and 60-62 and claim 1 at col. 4, line 47 to col. 5, line 7). The p+ diffusion depth of the source regions 29 is shallow relative to the p+ drain 27 diffusion and the source underdiffusion length, $U_s$, is less than the drain underdiffusion length, $U_d$. (Miller, Figure 6, col. 2, lines 3-6, col. 3, lines 34-36, lines 41-42 and lines 57-60 and claim 1 at col. 4, line 66 to col. 5, line 7).

## BACKGROUND

All claim rejections at issue in this appeal are made under 35 U.S.C. § 103(a)[1] The legal standards under 35 U.S.C. § 103(a) are well-settled.

Obviousness under 35 U.S.C. § 103(a) is a legal conclusion involving four factual inquiries:

(1) the scope and content of the prior art;

(2) the differences between the claims and the prior art;

(3) the level of ordinary skill in the pertinent art; and

(4) secondary considerations, if any, of non-obviousness.

Litton Systems, Inc. v. Honeywell, Inc., 87 F. 3d 1559, 1567, 39 U.S.P.Q. 2d 1321, 1325 (Fed. Cir. 196). See also Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office (PTO), the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); Manual of Patent Examining Procedure (MPEP), Edition 8(e8), August 2001, Sections 2142, 2143.03. "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 972 F.2d 1260 (Fed. Cir. 1992); In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988); In re Lalu, 747 F.2d 703,705, 223 U.S.P.Q. 1257, 1258 (Fed. Cir. 1984); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297 n.24, 227 U.S.P.Q. 657, 667 n.24 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 782 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). When a reference teaches away from the claimed invention, that teaching is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

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[1] "A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made." 35 U.S.C. §103(a).

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 USPQ.2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record." In re Lee, 277 F.3d 1338, 61 USPQ.2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant 's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ.2d 1430 (Fed. Cir. 1990). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" Lee (citing W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

## REJECTIONS

In the Final Office Action dated July 28, 2003, the Examiner rejected claims 18, 21-25 and 28-37 under 35 USC § 103(a) as being unpatentable over Kadosh in view of Miller.

For the reasons given below, the Appellant submits that the Examiner's rejection of the claims of Groups 1-3 (claims 18, 21-25 and 28-37) is improper and should be reversed.

**1. The claims of Groups 1-3 are patentable under 35 U.S.C. § 103(a) over Kadosh in view of Miller because the combination of Kadosh and Miller does not teach or suggest the Drain Extension is Deeper Than the Source Extension Limitation.**

Each of the independent claims 18, 21 and 31 recite a feature related to a drain extension and a source extension in which the drain extension is deeper than the source extension. This structure provides significant advantages. More particularly, the shallower source extension and deeper drain extension achieves at least three beneficial effects: 1) substantial immunity to short channel effects; 2) reduced peak electric field in the channel region reduces the possibility of hot-carrier injection into the gate oxide; and 3) higher drive current. (See Specification, page 3, lines 1-10). The shallower source extension allows the transistor to achieve control of short channel effects and higher drive currents and yet the

deeper drain extension allows the transistor to reduce hot carrier injection stress. (See Specification, page 5, line 15 to page 6, line 7).

In contrast, neither Kadosh nor Miller, in combination or alone, teaches or suggests a drain extension deeper than the source extension. The Examiner admits that Kadosh does not disclose a drain extension that is deeper than the source extension as required by independent claims 18, 21 and 31. Indeed, Kadosh shows a drain extension that is shallower than the source extension (Kadosh, Figure 1U). This is precisely the opposite structure to that recited in independent claims 18, 21 and 31.

The Examiner asserts that Miller teaches the limitation of a drain extension deeper than the source extension. In particular, in the Final Office Action, the Examiner states:

> . . . . Miller shows (fig. 6) a semiconductor device having a deep drain region (27) and a source region 29). The device includes source extension (underdiffusion region $U_s$) and a drain extension (underdiffusion region $U_d$) integral with the source and deep drain regions respectively. The drain extension is more than 80nm deep (col. 3, lines 15-19). The deeper drain extension provides an increased gate-drain capacitance (col. 3, lines 57-62) or vice versa (col. 4, lines 39-42). . . . Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the asymmetrical source/drain configuration of Kadosh by forming a drain extension deeper than a source extension as taught by Miller to increase the gate-drain capacitance.

---See Final Office Action at pages 2-3.---

> . . ., Miller was cited to show that a drain extension is deeper than a source extension. . . .[T]he examiner's interpretation that the portion of the source and drain under the gate of Miller (the portions labeled $U_s$ and $U_d$) which are labeled by Miller as underdiffusion regions, function as source and drain extensions. With that interpretation, the drain extension/underdiffusion portion is deeper than the source extension/underdiffusion portion. As seen in the drawings of the instant invention, the source and drain extension regions are formed directly under the sidewall insulators and outer portions of the gate electrode in the same manner as the underdiffusion portions of Miller. Miller does not use the term extensions" but because such underdiffusions are of the same structure and material as the extensions of the instant invent[illegible]

> underdiffusions function as extensions. Furthermore, the gate length and asymmetrical underdiffusions of Miller improve breakdown voltage characteristics of the silicon (col. 3, lines 57-67)."

However, as admitted by the Examiner, Miller does not provide any discussion of a source extension or a drain extension. In addition, the drain and source underdiffusion lengths, $U_d$ and $U_s$, are not of the same structure or function as the source and drain extensions of the present application. As discussed in the specification of the present application, the drain and source regions of a transistor may include a thin extension that is disposed partially underneath the gate to enhance transistor performance. (See Specification, page 1, lines 23-27). The source extension 23 and drain extension 25 are thinner than the deep source 22 and deep drain 24 regions and are disposed partially underneath a gate oxide 34. (See, Figure 1, Specification, page 5, lines 18-21 and page 5, line 30 to page 6, line 7). Accordingly, a source extension and a drain extension are regions of the source and drain that have a different depth that the deep source region 22 and deep drain region 24. (See, Figure 1, Specification, page 5, line 18 to page 6, line 1).

In contrast, the drain and source underdiffusion lengths, $U_d$ and $U_s$, disclosed in Miller are defined as the amount of overlap of gates 28 and the drain 27 and source 29 regions, respectively. See, Miller, Figure 6, col. 1, lines 29-32 and lines 34-37 and col. 3, lines 57-62). The underdiffusion lengths define the part of the source 29 and drain 27 under the gates 28. The sources 29 and drain 27 are comprised of a single doped region. In order to achieve a desired gate-drain capacitance, the entire drain region 27 is provided with a p+ diffusion depth which provides the desired drain underdiffusion length. (See, Miller, Figure 6, col. 2, lines 15-19 and col. 3, lines 9-17 and lines 60-62). As shown in Figure 6 of Miller, the entire drain region 27 including the portion of the drain region underneath the gate (e.g., defined by the drain underdiffusion length) has the same depth. Appellant also notes that Miller does not even include a discussion of spacers used in conventional extension implant processes. In addition, there is not teaching or suggestion in Miller of the functions of the source and drain extensions, such as, to achieve immunity to short channel effects, to reduce peak electric fields in the channel region, etc. The Examiner also asserted that the gate length and underdiffusions of Miller improve breakdown voltage characteristics of the silicon. However, Miller teaches that the gate may need to be lengthened because of the increased drain underdiffusion in order maintain a sufficient channel length to avoid voltage breakdown of the silicon. (See, Miller, col. 2, lines 21-25 and col. 3, lines 63-67).

Even if Kadosh and Miller could be properly combined, the combination of the cited art would not achieve the present invention. The combination of the teachings of Kadosh and Miller would result in a deep drain region that would be deeper than the deep source region of Kadosh. As discussed above, Miller does not teach or suggest a source extension or a drain extension. By combining the concepts of Kadosh and Miller, the deep drain region 198 of Kadosh would be increased in depth beyond the depth of the deep source region 206. A deeper drain extension would not be contemplated by one of ordinary skill in the art reviewing Kadosh and Miller.

As mentioned above, a prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP, Edition 8(e8), August 2001, Sections 2142, 2143.03. Even if Kadosh and Miller could be properly combined, these references do not teach or suggest the limitation that a drain extension is deeper than a source extension. Accordingly, the claims of Groups 1-3 are patentable over Kadosh in view of Miller.

**2. The claims of Groups 1-3 are patentable under 35 U.S.C. §103(a) over Kadosh in view of Miller because Kadosh teaches away from the Drain Extension is Deeper than the Source Extension Limitation.**

Teaching away from the claimed invention is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Kadosh clearly teaches away from the claimed invention.

As discussed above in section 1, Kadosh does not disclose or suggest the structure recited in independent claims 18, 21 and 31, in particular, the limitation that the drain extension is deeper than the source extension. Not only does Kadosh not provide a suggestion for this structure, Kadosh teaches precisely the opposite structure. Specifically, Kadosh teaches a method of making an asymmetrical N-channel or P-channel device with a drain extension 152 (or lightly doped drain region) which is shallower than the source extension 204. (Kadosh, Figure 1U).

Kadosh achieves the advantages of lower source-drain series resistance and reduced hot carrier effects by relying on a structure with a lightly doped drain, a heavily doped deep drain, a heavily doped source and ultra-heavily doped deep source. (Kadosh, col.

3, lines 7-15). If one of ordinary skill in the art used Kadosh in pursuit of the advantages mentioned by the Examiner, that person would fabricate an asymmetric transistor with a heavily doped deep drain and an ultra heavily doped deep source. In addition, the source extension would be deeper than the drain extension. Reducing the depth of source extension would not even be considered, especially when Kadosh clearly shows a deeper source extension. (Kadosh, Figure 1U) In addition, as discussed in detail in the Appeal Brief filed October 23, 2002, it would not have been obvious to one of ordinary skill in the art to interchange the drain and source regions. The source and drain are distinct structures that have completely distinct functions during the operation of a transistor. In particular, an asymmetric transistor structure, as described in Kadosh and the present application, includes a source and drain that are not identical structures and are not interchangeable.

Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Assuming *arguendo* that Miller suggested the modification of the lightly (p-) doped drain region 152 of Kadosh, the modification would result in a more heavily doped (p+) and deeper drain region 152, with the same depth as the heavily doped deep drain region (p+) 198 of Kadosh. While this structure may provide an increased gate-drain capacitance as taught by Miller, the modification would render the structure of Kadosh unsatisfactory for its purpose. As discussed above, Kadosh achieves the advantages of lower source-drain series resistance and reduced hot carrier effects by relying on a structure with a lightly doped drain, a heavily doped deep drain, a heavily doped source and ultra-heavily doped deep source where the drain extension is shallower than the source extension.

Accordingly, the claims of Groups 1-3 are patentable over the combination of Kadosh in view of Miller because Kadosh teaches away from the invention as recited in the claims of Groups 1-3.

**3. The claim of Group 3 is patentable under 35 U.S.C. §103(a) over Kadosh in view of Miller because the combination of Kadosh and Miller does not teach or suggest the dopant concentration limitations as recited in the claim of Group 3.**

Dependent claim 36 recites a unique concentration of dopants associated with the deep source and deep drain regions and the source extension and the drain extension. In particular, claim 36 requires that the deep source region and the deep drain region have the

the dopant concentrations and that the source extension, the shallow extension, has a higher concentration of dopants than the drain extension, the deeper extension. Even assuming, *arguendo*, that the Examiner's contention that the combination of Kadosh and Miller meets the limitations in the claims of the present application, the combination of Kadosh and Miller does not teach or suggest the limitations of claim 36. In contrast, Kadosh teaches the use of a deep source region having a different concentration of dopants than the deep drain region and a source extension, the deeper extension, having a higher concentration of dopants than a drain extension, the shallower extension. (Kadosh, Figure 1, col. 3, lines 29-33) In addition, Miller does not teach or suggest different concentrations of dopants within the drain region or source region. There is simply no suggestion for altering the concentration of dopants in Kadosh to meet the limitations of claim 36.

A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP, Edition 8(e8), August 2001, Sections 2142, 2143.03. Accordingly, the claim of group 3 is patentable over the combination of Kadosh in view of Miller which does not teach or suggest the dopant concentration limitations as recited in claim 36.

## CONCLUSION

In view of the foregoing, the Appellant submits that the claims are not properly rejected as being unpatentable under 35 U.S.C. § 103(a) under the cited reference. Accordingly, it is respectfully requested that the board reverse the claim rejections and indicate that a Notice of Allowance respecting all pending claims be issued.

Dated this 27th day of January, 2004

Respectfully submitted,

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## APPENDIX - THE CLAIMS ON APPEAL

18. An integrated circuit including a plurality of field effect transistors, each of the transistors comprising:

a gate structure disposed over a channel;

a deep source region heavily doped with dopants of a first conductivity type;

a deep drain region heavily doped with dopants of the first conductivity type;

a source extension integral the deep source region; and

a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension.

21. An integrated circuit includes a gate structure disposed over a channel, a deep source region heavily doped with dopants of a first conductivity type, a deep drain region heavily doped with dopants of the first conductivity type, a source extension integral the deep source region, and a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension, wherein the integrated circuit is manufactured by a method, comprising:

providing the gate structure between a source location and a drain location in a semiconductor substrate;

providing an angled source extension implant in a direction from the source location to the drain location;

providing an angled drain extension implant in a direction from the drain location to the source location; and

providing a deep source/drain implant at the source location and the drain location.

22. The integrated circuit of claim 21, further comprising providing a pair of spacers abutting lateral sides of the gate structure before the deep source drain implant.

23. The integrated circuit of claim 22, wherein the providing the source extension step is a low energy, high dose ion implantation step.

24. The integrated circuit of claim 23, wherein the drain extension implant step is a medium energy, high dose ion implantation step.

25. The integrated circuit of claim 24, wherein the source extension formed by the source extension step is shallower than the drain extension formed by the drain extension implant step.

28. The integrated circuit of claim 25, wherein the drain extension has a concentration between $1x10^{19}$-$5x10^{19}$ dopants per centimeter cubed.

29. The integrated circuit of claim 25, wherein the drain extension is more than 80 nm deep.

30. The integrated circuit of claim 27, wherein the gate structure is associated with a N-channel or P-channel with MOSFET.

31. An ultra-large scale integrated circuit including a plurality of field effect transistors, the field effect transistors comprising:

a gate structure on a top surface of a semiconductor substrate;

a source extension with dopants of a first conductivity type;

a drain extension with dopants of the first conductivity type; and

deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.

32. The integrated circuit of claim 31, further comprising:

a pair of spacers abutting lateral sides of the gate structure.

33. The integrated circuit of claim 31, wherein the drain extension is formed in a low dosage implant process.

34. The integrated circuit of claim 31, wherein the source extension is formed at an energy level of between 1-5 KeV.

35. The integrated circuit of claim 31, wherein the drain extension is formed at an energy level of between 5-15 KeV.

36. The integrated circuit of claim 31, wherein the deep source and deep drain regions have a concentration of dopants between $10^{19}$ and $10^{20}$ dopants per cc, the source extension has a concentration of dopants between $5x10^{19}$ and $10^{20}$ dopants per cc, and the drain extension has a concentration of dopants between $1x10^{19}$ and $5x10^{19}$ dopants.

37. The integrated circuit of claim 31, wherein the first conductivity type is P-type or N-type.